Three-Dimensional Masterslice MMIC on Si Substrate

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***Abstract*—This paper describes Si-based three-dimensional (3-D) monolithic microwave integrated circuit (MMIC) technology. This technology greatly improves the operating frequency of Si MMIC's up to the Ku band and makes them competitive with GaAs MMIC's in the higher frequency band. The characteristics of the coplanar waveguide formed on a lossy Si substrate and the TFMS line which is a basic element of the 3-D MMIC are numerically compared and discussed. An X-band amplifier, mixer, and highly integrated single-chip receiver using Si bipolar transistors are demonstrated to highlight the advantages of the Si 3-D MMIC technology. The cost reduction effect of the technology is also discussed. In our estimation, cost reduction of about 95% from conventional GaAs 2-D MMIC's can be achieved.**

***Index Terms*— Bipolar integrated circuits, finite-element methods, Masterslice, MMIC's, silicon devices, three-dimensional structures.**

I. Introduction

THE FORTHCOMING multimedia era will require highly integrated multifunctional monolithic microwave integrated circuits (MMIC's) for mobile communications, satellite communications, wireless LAN's, and so on. These applications will also require us to make the MMIC's cost effective. Si MMIC's have great advantages over GaAs MMIC's, such as a well-established fabrication process, lower process cost, and the potential for easy integration with digital large-scale integrated circuits (LSI's). In conventional Si IC design, differential pair transistors, Gilbert cells, and *R–C* coupled configurations are widely used. The operating frequency of these circuits is considerably low because the parasitic capacitance of the transistor degrades the high-frequency performance. Recently, several approaches have successfully implemented Si MMIC's into microwave applications, such as personal communication systems and wireless ATM, using on-chip inductors [1]–[4]. However, the operating frequency still remains at several gigahertz, due to its low substrate conductivity. Several approaches have tried to reduce the loss due to substrate conductivity by using a high-resistivity (several $\mathrm{k}\Omega \cdot \mathrm{cm}$) Si substrate [5], a thick dielectric film ($\sim$10 μm-thick) as an insulator or a microstrip line substrate [6], [7], shunted multilevel conductors with a large spacing between the conductors and Si substrate [8], or coplanar inductors [3].

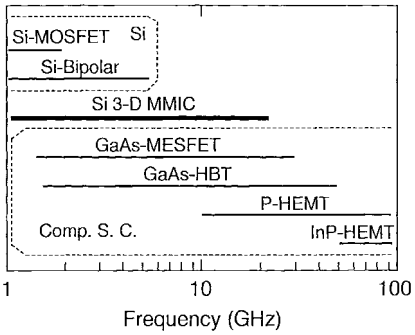

Fig. 1. Applicable frequency band of each device.

This paper describes a three-dimensional (3-D) MMIC technology [9]–[13] employing a Si substrate. The characteristics of a coplanar waveguide (CPW) formed on a lossy Si substrate and thin-film microstrip (TFMS) line which is a basic element of the 3-D MMIC are rigorously analyzed and compared using the finite element method. The TFMS line is far superior to the CPW in the high-frequency band and the Si 3-D MMIC technology allows us to use the reactive matching technique for Si MMIC design. By using this reactive matching technique, the operating frequency of Si MMIC's can be improved to nearly $f_{\max}/2$ as described in Section III. As a result, the Si 3-D MMIC technology greatly improves the operating frequency of Si MMIC's up to the Ku band using high $f_{\max}$ transistors such as SST1C [14] and makes them competitive with GaAs MMIC's in the frequency band, as shown in Fig. 1. The technology also greatly enhances the integration levels of MMIC's [12] and offers a Masterslice MMIC [13] that is a semi-custom MMIC similar to gate-array LSI's. Then, this technology effectively reduces the cost of MMIC's and wireless equipment.

II. Structure of the 3-D MMIC

The basic structure of the Si 3-D MMIC is shown in Fig. 2. Transistors, resistors, and lower electrodes of MIM capacitors

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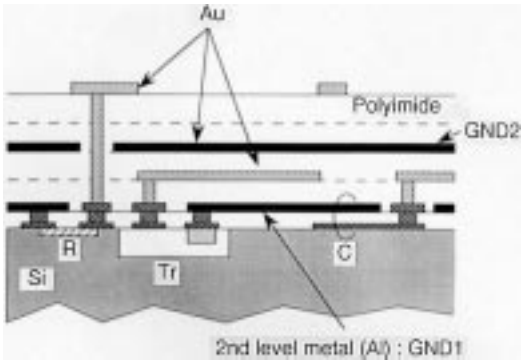


Fig. 2. Basic structure of the Si 3-D MMIC.

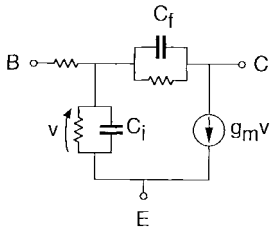
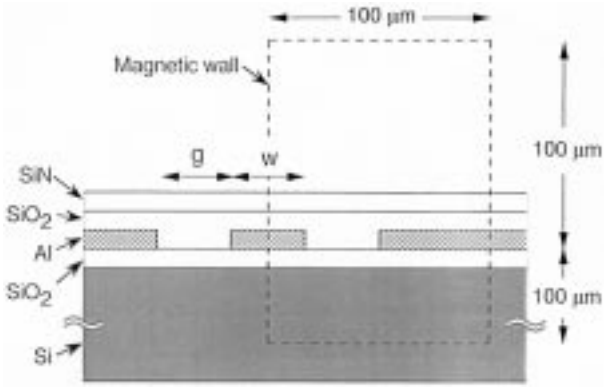
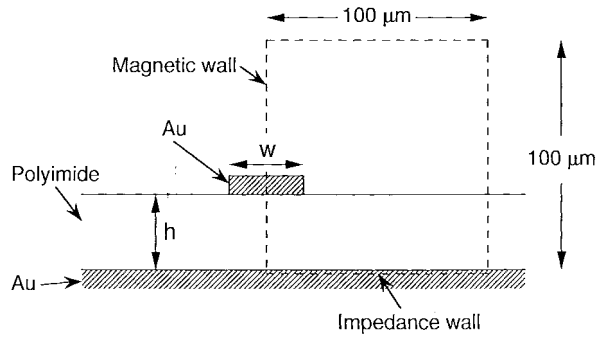


Fig. 3. Small-signal equivalent circuit of intrinsic bipolar transistor.



(a)



(b)

Fig. 4. Analyzed models of (a) CPW and (b) TFMS line.

are formed on a Si substrate and passivated. The second-level metal (Al) is formed on the passivation film and covers most of the wafer surface. The devices and the metals are formed using an ordinary Si IC process. After that, a 3-D passive structure constructed with four layers of 2.5-μm-thick polyimide film and four layers of 1-μm-thick Au metals (top conductor is 2 μm thick) is formed on the second-level metal. The fabrication process of the 3-D structure is almost the same as that of GaAs 3-D MMIC's [11]. The use of polyimide films offers good flatness even if the wafer has a rugged surface. The low-temperature process allows us to form 3-D passive circuits on many kinds of devices. Then the fabrication process can be used universally regardless of the kind of wafer. Contact resistance between Au and Al layers is better than 0.2 Ω per contact.

This structure also offers highly integrated multifunctional MMIC's and Masterslice MMIC's which are the same as those we demonstrated using a GaAs substrate in [12] and [13]. The high integration technology effectively enhances the integration to a level three to five times that of conventional 2-D MMIC's. The 3-D Masterslice MMIC technology reduces development turn-around-time (TAT) and fabrication cost. It also eliminates the high-level design skill necessary for MMIC design.

III. Operating Frequency

The unit-stage voltage gain of an *R–C* coupled amplifier is expressed in

$$G_v \simeq \frac{-g_m}{1/Z_L + j\omega C_f} = \frac{-g_m R_L}{1 + j\omega R_L (C_f + C_i)}$$

using equivalent circuit parameters shown in Fig. 3, where load impedance Z_L is assumed to be a parallel connection of load resistance R_L and input capacitance C_i of the next stage. Then the gain (G)-bandwidth (B) product of the amplifier is given by

$$G \cdot B = \frac{g_m}{2\pi(C_f + C_i)}.$$

It is well known that the GB product of a negative feedback amplifier is the same as that of a simple *R–C* coupled amplifier. Since f_T is also expressed in

$$f_T \simeq \frac{g_m}{2\pi(C_f + C_i)}$$

the bandwidth of the simple *R–C* coupled amplifiers and negative feedback amplifiers cannot be extended above the line $G' \cdot B = f_T/\sqrt{2}$, where G' is the gain decreased by 3 dB from the flat gain G. As a result, the operating frequency of the amplifier is around $f_T/5$–$f_T/3$. On the other hand, reactive matching circuits are usually used to achieve the maximum available gain (MAG) limited by $f_{\max}$ at the upper band edge in the microwave and millimeter-wave bands. Then, the operating frequency of the reactive matching amplifier achieves a level from $f_{\max}/3$–$f_{\max}/2$. In the conventional Si MMIC design, the reactive matching technique cannot be effectively used because of the lack of high Q inductors and transmission lines due to nonnegligible substrate conductivity.

TABLE I
THICKNESS AND PROPERTY OF EACH LAYER

Coplanar waveguide (CPW)		
SiN layer	0.7 μm	$\varepsilon_r = 7.9$
SiO_2 layer	0.5 μm	$\varepsilon_r = 3.9$
2nd Al layer	1.0 μm	$\sigma = 3.08 \times 10^7$ S/m
SiO_2 layer	0.7 μm	$\varepsilon_r = 3.9$
1st Al layer	0.5 μm	$\sigma = 3.08 \times 10^7$ S/m
SiO_2 layer	1.7 μm	$\varepsilon_r = 3.9$
Si substrate	625 μm	$\varepsilon_r = 11.7$
		$\rho = 30\,\Omega \cdot$ cm
TFMS line		
Top Au layer	2.0 μm	$\sigma = 4.10 \times 10^7$ S/m
Polyimide layer	4 μm/9 μm	$\varepsilon_r = 3.3$
Ground Au layer	∞	$\sigma = 4.10 \times 10^7$ S/m

This is the reason why Si MMIC's are not available in the higher frequency band.

IV. CHARACTERISTICS OF TRANSMISSION LINES

A. Finite Element Method

In order to examine the characteristics of metal–insulator–semiconductor structure CPW's and TFMS lines, conductor loss and substrate loss must be accurately evaluated. Moreover, the thickness of the conductors must be considered because the thickness is not much thicker than skin depth in the lower frequency region. Thus we adopted the full wave vector finite element method (FEM) [15]. The finite element formulation is derived from the four components of transverse electromagnetic field using the Galerkin method, and discretized with quadratic vector shape functions. Dielectric loss and conductor loss are rigorously taken into account by using a complex permittivity. The thickness of the conductors, i.e., the skin effect, is also accurately considered.

Analyzed models for the CPW and TFMS line are illustrated in Fig. 4. The thickness and property of each layer are shown in Table I. The center conductor and slot widths of the CPW are w and g, respectively. The conductors are made of aluminum (Al) which is ordinarily used in conventional Si IC process. A SiO_2 layer is sandwiched by the conductor layer and the Si substrate, and a SiO_2 layer and SiN layer are overlaid on the conductor layer. The TFMS line is constructed with stacked polyimide films, strip conductor, and ground metal. Gold (Au) is used as a conductor in the 3-D process. The width of the strip conductor and the thickness of polyimide film are w and h, respectively. In the analysis, the polyimide is assumed to be lossless, and the ground metal is assumed to be infinitely thick for simplicity. However, the difference between the characteristics of the TFMS lines with 1-μm-thick ground plane and infinitely thick ground plane was less than 1%.

The dashed line rectangles in Fig. 4 show the analyzed region of each transmission line. The analyzed region is a half plane of each transmission line cross section because of its structural symmetry. The region is surrounded by magnetic walls (the ground plane of the TFMS line is an impedance wall), and divided into about 200 and 100 elements for the CPW and TFMS line, respectively.

The calculated results of this method were compared with the measured and calculated results shown in [16], and good agreement has been obtained.

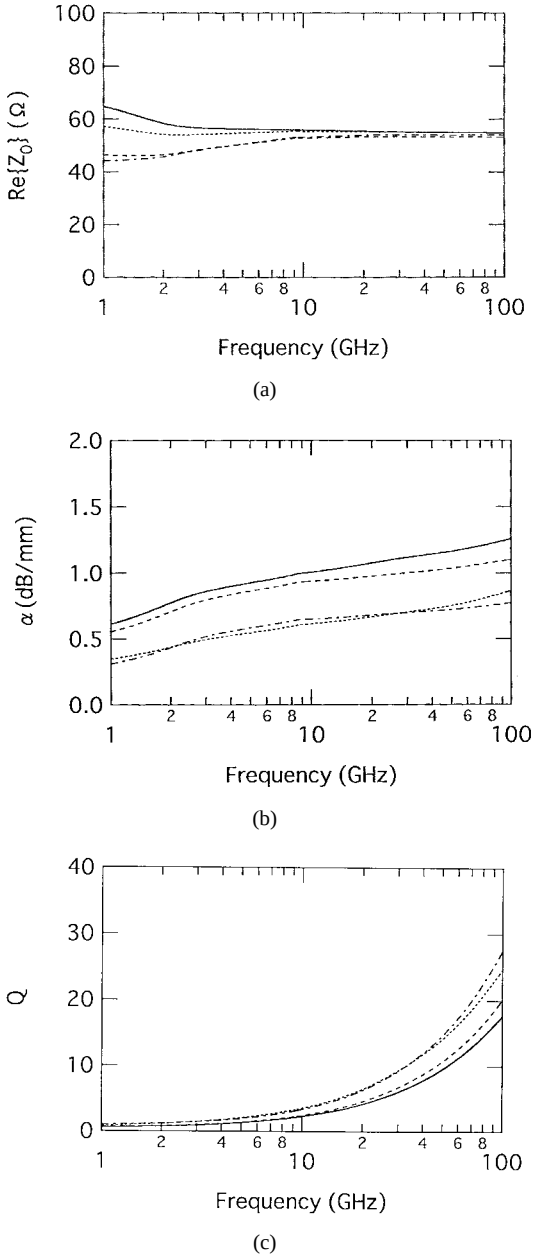


Fig. 5. Calculated characteristics of the CPW's (—: $w = 10$ μm, $g = 5$ μm with AL1; - - -: $w = 20$ μm, $g = 10$ μm with AL1; $\cdots\cdots$: $w = 10$ μm, $g = 5$ μm with AL2; and -·-·-: $w = 20$ μm, $g = 10$ μm with AL2). (a) Characteristic impedance, (b) attenuation constant, and (c) Q factor.

B. CPW

Fig. 5 shows the calculated characteristics of the four types of CPW's. The solid line shows the results of the CPW made of the first Al layer (AL1) whose widths are $w = 10$ μm, $g = 5$ μm. The dashed line shows the results of the CPW made of

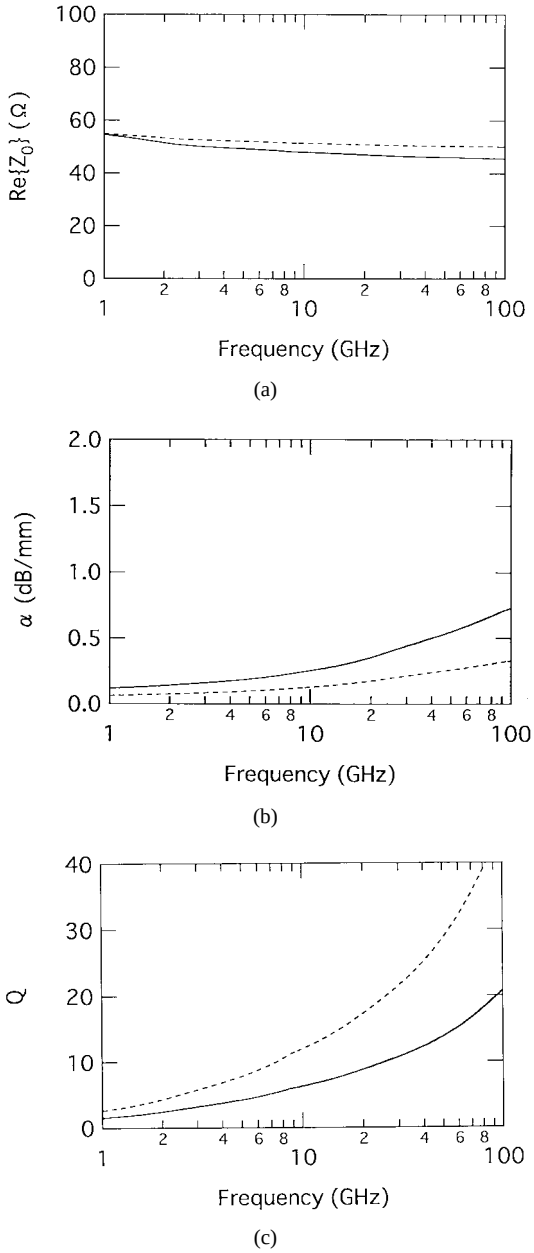


Fig. 6. Calculated characteristics of the TFMS lines (—: $w = 10\ \mu$m, $h = 4\ \mu$m; and - - -: $w = 20\ \mu$m, $h = 9\ \mu$m). (a) Characteristic impedance, (b) attenuation constant, and (c) Q factor.

AL1 whose widths are $w = 20\ \mu$m, $g = 10\ \mu$m. The dotted line shows the results of the CPW made of the second Al layer (AL2) whose widths are $w = 10\ \mu$m, $g = 5\ \mu$m. The chained line shows the results of the CPW made of AL2 whose widths are $w = 20\ \mu$m, $g = 10\ \mu$m. Fig. 5(a)–(c) shows the real part of the characteristic impedance, attenuation constant α, and Q factor defined as $Q = \pi/\lambda_g\alpha$, where λ_g is the wavelength of the guided wave. The characteristic impedance of each CPW is around 50 Ω. The attenuation constants of the CPW's using the first Al layer are much higher than those of the CPW's using the second Al layer. The difference is due to the difference in the thickness of both the Al layer and the insulator layer between Al and the Si substrate. The

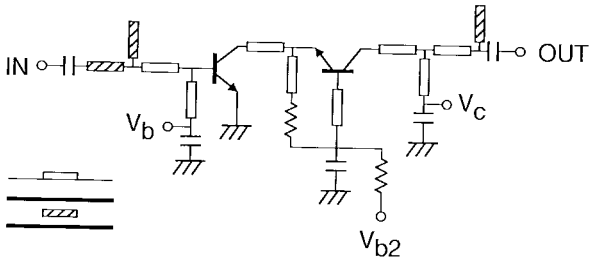


Fig. 7 Circuit scheme of the fabricated X-band amplifier using cascode Si bipolar transistors.

Q factor of each CPW is less than 5 in the frequency range between 1–20 GHz. These results show that it is difficult to obtain reasonable reactive matching circuits using CPW's in the frequency range.

C. TFMS Line

Fig. 6 shows the calculated characteristics of the TFMS lines. The solid and dashed lines show the results of the TFMS line with $w = 10\ \mu$m, $h = 4\ \mu$m and $w = 20\ \mu$m, $h = 9\ \mu$m, respectively. Fig. 6(a)–(c) shows the corresponding results to Fig. 5(a)–(c). The characteristic impedance of each TFMS line is also around 50 Ω. The attenuation constants are less than 0.3 dB/mm around 10 GHz and much less than those of the CPW's. The Q factors of 10 μm- and 20 μm-wide TFMS lines are about 7 and 12 around 10 GHz, respectively. The Q factors are high enough to achieve the reactive matching circuits in this frequency. There are three reasons why the TFMS line has low loss characteristics. The first is that the ground plane of the TFMS line effectively isolates the wafer property, such as conduction, to the line characteristics. The second is that the strip conductor is made of Au which has a higher conductivity than Al. The last is that the thickness of the strip conductor is twice as thick as that of AL2 CPW. However, the Q factor of TFMS line still remains better than 7 when $w = 20\ \mu$m even if the strip conductor is made of Al and its thickness is 1 μm.

V. Circuit Design and Performance

By using the second-level metal shown in Fig. 2 as a ground plane (GND1), the conductive property of the wafer is effectively isolated from passive structures created on GND1, and high Q passive circuits are available as shown in the previous section. This allows the use of a reactive matching technique for Si MMIC design and greatly improves the operating frequency of the Si MMIC's.

A. Amplifier

We first examined the X-band amplifier shown in Fig. 7. The ground plane of the second-level metal (GND1), which separates the wafer and the 3-D passive circuits, enables Si MMIC's to be designed in the same way as GaAs MMIC's. The amplifier is constructed with cascode Si bipolar transistors (SST1C [14]), TFMS lines, and triplate thin-film striplines for reactive matching. The TFMS lines and striplines are stacked

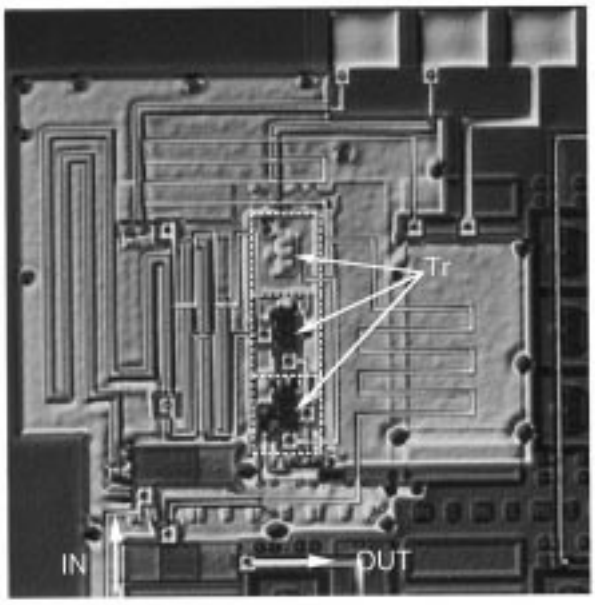


Fig. 8. Microphotograph of the fabricated X-band amplifier.

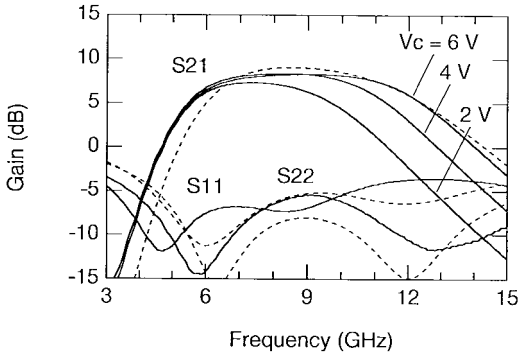


Fig. 9. Measured performance of the fabricated X-band amplifier. Measured performance (—) and predicted performance (- - -) when $V_c = 2$ V.

to reduce the circuit area. The widths of the TFMS lines and triplate striplines are 10 μm and 11 μm with the characteristic impedance of 50 Ω and 20 Ω, respectively.

Fig. 8 shows a microphotograph of the amplifier fabricated using 3-D masterslice MMIC technology. Three transistors, resistors, and lower electrodes of MIM capacitors are formed on a wafer in advance, and two transistors are used. The single-stage amplifier occupies only a 0.73 mm $\times$ 0.77 mm area. Fig. 9 shows the measured and predicted performance of the fabricated amplifier. The solid line shows the measured performance and the dashed line shows the simulated value. Although this is the first trial and we did not have any good device models for the high-frequency region, reasonable agreement between them has been obtained. A gain of 8 dB is obtained over 7–10 GHz at a collector voltage $V_c = 4$ V (2 V for each transistor) and the operating frequency achieves 12 GHz at $V_c = 6$ V. Each transistor has nine 0.3 $\times$ 13.4 μm emitters and the measured $f_{\max}$ is around 30 GHz at $V_{ce} = 1$ V because the transistor is a multi-emitter transistor for analog

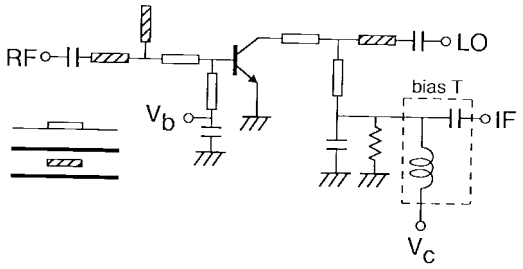


Fig. 10. Circuit scheme of the fabricated X-band mixer using Si bipolar transistor.

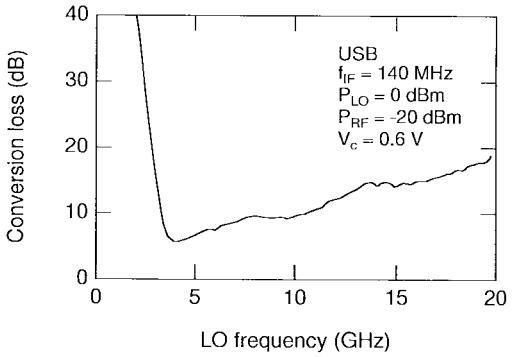


Fig. 11. Measured performance of the fabricated X-band mixer.

application (40 GHz for digital). The operating frequency nearly achieves $f_{\max}/3$.

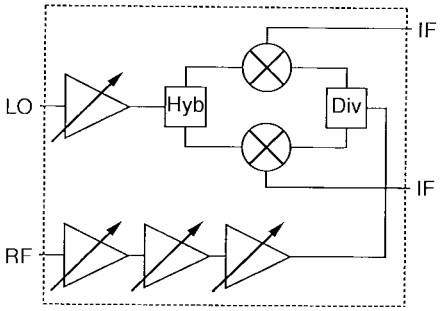
B. Mixer

Fig. 10 shows a circuit scheme of the X-band mixer. The mixer employs a common-emitter transistor and a collector LO injection configuration. An RF signal is fed into the transistor from the base electrode, and an IF signal is emitted from the collector electrode. Matching circuits are constructed with TFMS lines and triplate thin-film striplines and are optimized for the RF and LO frequencies, respectively. The RF and LO matching circuits are stacked above and below the ground metal located in the middle of the polyimide layer.

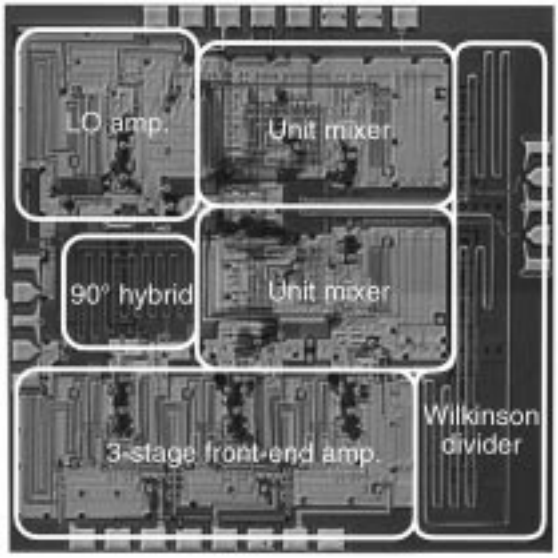
Fig. 11 shows the measured performance of the fabricated mixer. Conversion loss of better than 10 dB is obtained over a wideband frequency range from 5 to 10 GHz, where the LO and RF power are 0 and -20 dBm, respectively. The IF frequency is 140 MHz, and $V_c = 0.6$ V.

C. Single-Chip Receiver

Fig. 12 shows a block diagram and a microphotograph of the fabricated X-band highly integrated single-chip receiver which includes a three-stage front-end amplifier, an LO amplifier, and an image-rejection mixer in a 2.3 $\times$ 2.3 mm chip. The image-rejection mixer is constructed with two unit mixers, a Wilkinson divider employing TFMS lines, and a quadrature hybrid employing a multilayer broad-side coupler [9]. The amplifiers and unit mixers are described in the previous sections. By using meander-like configurations, a compact layout has been achieved. Fig. 13 shows the measured performance of the fabricated single-chip receiver. A 15–20-dB gain and better



(a)



(b)

Fig. 12. Fabricated X-band single-chip receiver including a three-stage front-end amplifier, an LO amplifier, and an image-rejection mixer in a 2.3 × 2.3 mm chip. (a) Block diagram. (b) Microphotograph.

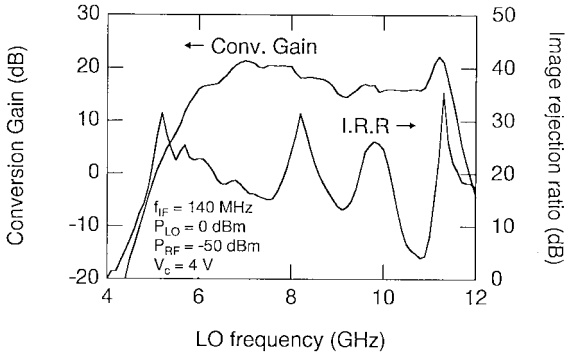


Fig. 13. Measured performance of the fabricated single-chip receiver.

than 20-dB image-rejection ratio are obtained in the X-band, where the LO and RF power are 0 and −50 dBm, respectively. The IF frequency is 140 MHz.

VI. Cost Reduction

Cost estimation of the Si 3-D MMIC is shown in Fig. 14 compared with conventional 2-D GaAs MMIC's. The 3-D and Masterslice MMIC technologies reduce cost by more than 50% due to its high integration level even if an additional

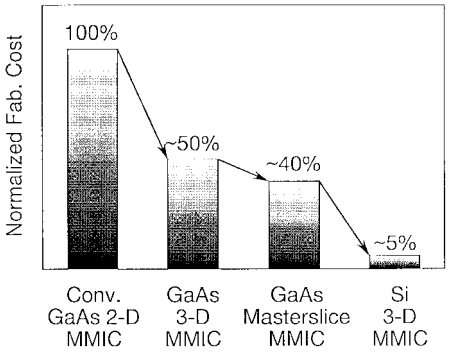


Fig. 14. Estimated cost-reduction effect of Si 3-D MMIC.

3-D process is necessary. The Masterslice technology further reduces the fabrication cost because the masterslice substrate can be mass produced (and the TAT is much shorter) while still maintaining a high integration level. Finally, Si 3-D MMIC's effectively have a lower cost due to their lower process costs and larger wafers. The result is a cost reduction of about 95% from conventional GaAs 2-D MMIC's.

VII. Conclusion

The 3-D MMIC technology greatly improves the operating frequency of Si MMIC's up to the Ku band and makes them competitive with GaAs MMIC's in the frequency band. The Si 3-D MMIC's using BJT's, CMOS's, and BiCMOS's also have the potential to be easily integrated with digital LSI's as well as having a low cost. This technology promises to achieve cost-effective intelligent wireless communication systems and will take us into the forthcoming multimedia era.

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Ichihiko Toyoda (M'91), for a photograph and biography, see this issue, p. 2443.

Kenjiro Nishikawa (A'93), for a photograph and biography, see this issue, p. 2315.

Tsuneo Tokumitsu (M'88), for a photograph and biography, see this issue, p. 2443.

Kenji Kamogawa (M'93), for a photograph and biography, see this issue, p. 2443.

Chikara Yamaguchi, for a photograph and biography, see this issue, p. 2443.

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